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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,129	03/31/2004	Yoshihisa Hiramatsu	103213-00076	3718

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EXAMINER	
NGUYEN, HIEP	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 12/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/813,129	<b>Applicant(s)</b> HIRAMATSU ET AL.	
	<b>Examiner</b> Hiep Nguyen	<b>Art Unit</b> 2816	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 03 October 2005.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### DETAILED ACTION

This is responsive to the amendment filed on 10-03-05. Applicant's arguments with respect to admitted prior art have been carefully considered but they are not deemed to be persuasive. Thus, the claims remained rejected under the prior art.

#### *Specification*

The disclosure is objected to because of the following informalities: then disclosure "(0015)... When the voltage applied to the input terminal 1 is lower than a threshold level Vs, the potential difference across the resistor R2 is so low that the transistor Q1 is kept on and the transistor Q2 is kept off" is misleading because voltage (Vs) is the input signal, not the threshold. The threshold is a "predetermined value" of (Vs) that makes diode (Q3) conductive and a low voltage is applied to the gate of transistor (Q1). According to figure 1 of the present application, the voltage that is applied to the gate of transistor (Q2) is lower than the voltage applied to the gate of transistor (Q1), thus when transistor (Q1) is turned on, transistor (Q2) is turned on also at the same time.

Appropriate correction is required.

#### *Claim Objections*

Claims 1 and 13 are objected to because of the following informalities: the recitations "a fourth resistor" in claim 1 and "the serial circuit" in claim 13 lacks antecedent basis. The 1-3 resistors are not recited. Appropriate correction is required.

#### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

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Regarding claims 1, 7 and 13, the recitation “wherein whether the input voltage is equal to a predetermined level or not is checked based on an output from the differential pair” is indefinite because it is misdescriptive. Figure 1 of the present application shows that when the input voltage (Vs) is lower enough so that diode (Q3) is not conductive, no current is flowing through the voltage division circuit and the gate of transistor (Q1) is pulled to ground level and transistor (Q1) is turned on. Thus, when the input voltage (Vs) is equal to a predetermined level or not (lower than a predetermined level) transistor (Q1) is turned on. Voltage (Vs) is **the input voltage**, not the predetermined voltage as argued in the Remarks.

Regarding claims 5, 11 and 15, the recitations “the predetermined voltage is equal to a sum of a first multiplication product and a second multiplication product”, “a value by dividing a sum of the resistance of the third resistor and a resistance of the resistor by the resistance of the resistor”, “the first multiplication product”, “a value” on line 9, “the second multiplication product”, “a value” on line 13 are indefinite because it is not clear what they are meant by. The Applicant is requested to clearly show how the “predetermined voltage”, “the first multiplication product”, “a value” on line 9, “the second multiplication product” and “a value” on line 13 of claim 5 are calculated. The same rationale is applied to claims 11 and 15.

Claims 2, 4, 6, 8-10, 12 and 14 are indefinite because of the technical deficiencies of claims 1, 7 and 13.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 6, 7, 9, 10 and 12-14 are rejected under 35 U.S.C. as being anticipated by the admitted prior art.

Regarding claims 1, 6 and 7, the prior art, figure 1, shows a voltage detection circuit comprising: first and second transistors (Tr5, Tr4), a voltage division circuit (r1-r4, Tr1)

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being connected directly to the base of transistor (Tr5) and transistor (Tr4), a resistor (r5) connects the base of transistor (Tr4) to the emitter of transistor (Tr4). The input voltage is checked when the input voltage is high enough to turn the transistors on. The output transistor is a transistor that has the collector connected to output terminal (4) wherein a reset signal is generated. Note that the voltage division circuit comprises resistor (r4) thus; the voltage division circuit is connected directly to the base of the first transistor (Tr4).

Regarding claims 9, 10 and 12, the serial circuit is circuit (Tr1, r3) and the bases of transistors (Tr4, Tr5) are connected to the resistor network as shown in figure 4. The voltage across the rectifying element (Tr1) is equal to the voltage across the base-emitter of the second transistor (Tr4) because they are both equal to a diode drop. The output transistor is transistor that has the collector connected to output terminal (4) wherein a reset signal is generated.

Regarding claims 13 and 14, the prior art, figure 1, clearly shows a method for fabricating a semiconductor integrated circuit device as called for in claim 13. The input voltage is applied to the voltage division circuit comprising serially connected resistors and diode connected transistor (r1-r4, Tr1) and inherently these components are formed in the IC simultaneously by a same process. The voltage across the rectifying element (Tr1) is equal to the base-emitter of the second transistor (Tr4) because they are both equal to a diode drop.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2-4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art.

Regarding claims 2 and 8, the prior art includes all the limitation of claims 2 and 8 except for the limitation that the first and second transistors are PNP transistors. However, it

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is well known in the art that PNP and NPN transistors are interchangeable for conforming to the input voltage and the power supply voltage. Therefore, it would have been obvious to an artisan having skills in the art to replace NPN transistors of the prior art with PNP transistors for conforming to the input voltage and the power supply voltage.

Regarding claim 3, and 4, the prior art shows a voltage division circuit (r1-r4, Tr1). The output voltage is equal to a predetermined voltage and the voltage across the rectifying element (Tr1) is equal to the base-emitter of the second transistor (Tr4) because they are both equal to a diode drop.

### *Response to Arguments*

In the Remarks, page 12, the Applicant argues that “and therefore the threshold value is NOT  $V_{f1}$  but rather  $V_s$ ”. This is not persuasive because ( $V_s$ ) is an input voltage. The threshold value is a voltage value of ( $V_s$ ) that makes diode (Q3) conductive. If the input signal ( $V_s$ ) is equal or less than the “threshold value”, both transistors (Q1) and (Q2) are turned on because the voltage applied to the base of transistor (Q2) is always smaller than the voltage applied to the gate of transistor (Q1). Note that when the input voltage ( $V_s$ ) is less than the “threshold voltage”, diode (Q3) is not conducting, both bases of transistors (Q1) and (Q2) are pulled to ground and they are both turned on. Thus the recitation “wherein whether the input voltage is equal to a predetermined level or not is checked based on an output from the differential pair” is not clear.

### *Conclusion*

Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

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however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen

12-06-05



TUAN T. LAM  
PRIMARY EXAMINER